REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official Action dated 30 December 2004. Responsive to the rejections made in the Official Action, Independent Claim 1 has been amended to clearly distinguish the present invention from the references cited by the Examiner. Claim 1, as well as Dependent Claims 3, and 5-7, have additionally been amended to improve the Claim language thereof. Claim 2 has been canceled without prejudice to incorporate the subject matter thereof into the Claim 1 and Claim 4 has been canceled without prejudice or disclaimer of the subject matter thereof.

Prior to a review of the references cited by the Examiner, it is believed that a brief discussion of the present invention is in order to facilitate the understanding of the inventive concept thereof. As such, the present invention is related to an improved structure of gold fingers, known as bonding pads, in a stacked-chips packaging arrangement. The stacked chip package includes a packaging substrate and a plurality of chips stacked upon the packaging substrate. Each chip has at least one wire to be connected to a chip wire of other stacked chips.

Bonding pads, or improved gold fingers of the present invention, are implemented as gold finger sets (gold finger unit arrays) each of which includes an array of gold finger units electrically connecting each to the other by a conductive material extending therebetween and separated into positionally distinct gold finger units by a solder resist

structure which extends therebetween and on the top of the conductive material of the gold finger set. In such arrangement, each chip wire of the plurality of stacked chips is coupled to a respective one of the gold finger units. Those chip wires which are to be connected together are connected to the distinct gold finger units of the same gold finger set. In this manner, as explained in detail in the Specification of the present Patent Application, the problems associated with the prior gold fingers known in the art, such as difficulties with chip wires bonding experienced in the stacked chips packaging, are overcome by the arrangement of the gold finger sets of the present invention.

In the Official Action, Claims 1-6 were rejected under 35 U.S.C. § 102(b) as being anticipated by Spielberger, et al., U.S. Patent #6,005,778, and Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Spielberger, et al. in view of Rumsey, U.S. Patent #6,356,452.

Spielberger, et al., the primary reference cited by the Examiner, is directed to a chip stacking arrangement which includes a substrate 14 on the top of which a plurality of chips are stacked. The substrate 14 includes bonding pads 18 for making an electrical connection to package conductive paths. The electrical connections between the chips and the substrate are formed of thin wires 28 having a wire bond connection at packaging bond pads 18. As shown at the left-hand side of Fig. 1, the wires 28 of each chip 20 and 40 are connected to separate bond pads 18, and as shown at the right-hand side of Fig. 1, the wires 28 are bonded to the same pad 18.

It is respectfully submitted that Spielberger, et al., fails to disclose, suggest, or render obvious the structure which the Applicant regards as the invention. Specifically,

A. As shown at the left hand side of Fig. 1, the wires of each chip 20 and 40 are coupled to separate bonding pads 18. However, these bonding pads 18 are not a part of the gold finger array and are not electrically connected each to the other. Therefore, the chip wires coupled between the chips and these electrically separated pads 18 are not coupled each to the other.

In the present invention the improved gold finger arrangement includes a plurality of gold finger units electrically connected one to the other to form the gold finger set (array). The chip wires are coupled each to the other being bonded to the gold finger units of the same gold finger set. This feature is completely missing from Spielberger, et al.

B. In Spielberger, et al., as opposed to the present invention only the wires 28 at the right-hand side of Fig. 1 are connected one to the other. However, they all are coupled to the same bonding pad 18 as is customary in the art of stacked chip packaging arrangements. Such a design has bonding problems discussed on Pages 1-2 of the subject Patent Application which are overcome by the improved gold finger structure of the present invention.

Opposingly in the present invention the chip wires which are to be connected one to the other are coupled each to a distinct gold finger unit of the same gold finger set. In

the gold finger set, the distinct gold finger units are positionally separated each from the other by the solder resist structure to overcome bonding problems associated with coupling of all chip wires to the same bond pad as shown in Fig. 1 (on the right-hand side). This feature is completely missing from Spielberger, et al.

Spielberger, et al., contrary to the present invention, fails to either separate the bonding pad 18 (at the right-hand side of Fig. 1) into distinct gold finger units for connection thereto of the chip wires 28 (each wire to a respective positionally distinct gold finger unit), or to electrically connect the bonding pads 18 (at the left-hand side of Fig. 1) and to positionally separate these bonding pads 18 by a solder resist structure, covering the electrical connection. Therefore, this reference is dramatically distinct from the structure which the Applicant regards as the invention and as claimed in now amended Independent Claim 1. As amended, Claim 1 now emphasizes that each gold finger set includes a plurality of gold finger units electrically connected to one another by a conductive material and positionally separated one from another by a solder resist structure extending above said conductive material, and wherein the chip wires of the plurality of chips to be connected to one another are connected to the distinct gold finger units of the same gold finger set.

It is respectfully submitted that as Spielberger, et al. fails to disclose each and every one of the elements of the invention of the subject Patent Application, as now claimed in Claim 1, does not anticipate the invention of the subject Patent Application

and the subject Application is not obvious in light thereof. Therefore, Claim 1, as amended, is believed to contain the allowable subject matter and the allowance of Claim 1 is respectfully urged.

The Rumsey reference cited by the Examiner is a multi-layer circuit board which includes a base layer, conductive layer, and a solder mask. The solder mask layer has two sets of openings, one of the sets of openings are vent openings that expose the base layer to permit the gases to escape during processing. The second set of openings expose selective regions of a conductive layer. As described, the conductor openings 130, shown in Figs. 1 and 2, permit exposure of selected areas of the conductor. Additionally, as shown in Figs. 3 and 4, the solder mask layer 320 has openings to provide access to the grid array conductors 360 and second openings 340 are provided to expose the base layer. However, none of the openings 130 or 360 are described as bond pads in the Rumsey Patent. The only bond pads shown in the structure of Fig. 3 are the bond pads 325 which are located at the region 330 of the circuit board external the aperture 310.

It is respectfully submitted that the Rumsey reference fails to suggest, describe, or render obvious the structure which the Applicant regards as the invention. Specifically,

A. The structure of Rumsey, specifically the die 460, is not a stacked chip packaging structure and therefore, it is not concerned with bonding of the wires of stacked chips to bond pads 325.

In the present invention, the packaging arrangement is a stacked chip packaging structure which includes a plurality of stacked chips with chip wires bonded to the gold fingers in a predetermined order.

B. The present invention, in contrast to Rumsey, discloses gold finger units which are arranged in sets where each gold finger unit is connected each to the other by a conducting material and positionally separated one from another in order to couple chip wires of the plurality of stacked chips to positionally distinct gold finger units of the same gold finger set. These elements are completely missing in Rumsey.

It is respectfully submitted that there is no motivation to combine Rumsey (which is not a stacked chip packaging structure and which is not concerned with arranging of bonding pads 325 in sets (or clusters) of the bonding pads to improve the coupling of the chip wires thereto) with Spielberger, et al., (which couples the chip wires of the stacked chips to the same bonding pad or to different bonding pads which however are not electrically connected). It is not believed that the subject Patent Application can be made obvious when the Claims, as amended, are carefully reviewed.

Arguendo, even if the teachings of the cited references, Spielberger, et al. and Rumsey, are combined, none of them taken singly or in combination thereof disclose, suggest, or render obvious the stacked chip packaging structure which includes a plurality of gold finger sets, wherein each gold finger set includes a plurality of gold finger units electrically connected to one another by a conductive material and positionally separated

one from another by a solder resist structure extending above the conductive material, and wherein the chip wires of the plurality of the stacked chips to be connected one to another are connected to the gold finger units of the same gold finger set with each chip wire connected to a positionally distinct gold finger unit.

It is believed that the claimed combination of elements provides patentable distinction over the structure resulting from the Examiner's suggested combination of Spielberger, et al. and Rumsey. As Claim 1 directs itself to the concept and structure of the stacked chip packaging arrangement comprising a plurality of chips stacked on the packaging substrate, and a plurality of gold finger sets positioned on the packaging substrate, wherein each gold finger set includes a plurality of gold finger units electrically connected to one another by a conducting material and positionally separated one from another by a solder resist structure extending above the conductive material, and wherein the chip wires of the plurality of stacked chips to be connected one to the other are connected to the gold finger units of the same gold finger set, with each chip wire connected to a distinct gold finger unit, it is believed to show patentable distinction over the cited prior art whether the references are taken singly or in combination. Accordingly, Claim 1 as amended is believed to be allowable and such action is respectfully requested.

Claims 3, and 5-7, are believed to be patentably distinct over the cited prior art for at least the same reasons as provided for Claim 1 which is now believed to be an

allowable base Claim. The allowance of Dependent Claims 3 and 5-7 is respectfully urged.

For all of the foregoing reasons, it is now believed that the subject Patent Application has been placed in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

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Dated: 3/29/05

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